ISSN: 0975-8585

Research Journal of Pharmaceutical, Biological and Chemical Sciences

Performance Analysis of High Efficient CAM Using Parity Bit and Gated Circuits.

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ABSTRACT

Content Addressable Memory (CAM) is a type of solid-state memory which is used to access the address of the given data from the memory banks whereas, the ordinary memory provide the data of the specified address. CAM offers high speed in a single clock cycle .The input given to CAM is data. The data carried to the CAM cell with the help of match line and it retrieves the address of the specified data. The techniques used are parity bit and gated power. Parity bit technique which serves at faster rate by reducing its delay. Peak power consumption can be reduced by using gated power technique. The technology in CAM can be of 45-nm.The average power consumed using CMOS technology can be of 4.43*10^-6.CAM finds its application on database engines, database hardware compression.

Keywords: Content Addressable Memory (CAM), Match-Line (ML).

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ISSN: 0975-8585

INTRODUCTION

With the small and effective transistors at their hands, electrical engineers of the 50s saw the possibilities of constructing f9ar more advanced circuits than before. However, as the complexity of the circuits grew, problems started arising, mainly with the size of the circuits. A complex circuit, like a computer, was depended on speed. If the components of the computer were too large or the wires interconnecting them are too long, the electric signals couldn't travel fast enough through the circuit, thus making the computer too slow to be effective. As microprocessors become more complex due to technology scaling, microprocessor designers have encountered several challenges which force them to think beyond the design plane and they are Inorder to maintain logic complexity, the design should scale down to reduce the area. As area decreases, heat dissipation increases thus power dissipation also increases.There should be trade-off between power consumption and area.As photolithography techniques tend closer to the fundamental laws of optics, achieving high accuracy in doping concentrations and etched wires is becoming more difficult and prone to errors due to variation. Designers now must simulate across multiple fabrication process corners before a chip is certified ready for production.Use to lithography and etch issues with scaling, design rules for layout have become increasingly stringent. Designers must keep ever more of these rules in mind while laying out custom circuits. The overhead for custom design is now reaching a tipping point, with many design houses opting to switch to Electronic Design Automation (EDA) tools to automate their design process.As clock frequencies tend to scale up, designers are finding it more difficult to distribute and maintain low clock skew between these high frequency clocks across the entire chip. This has led to a rising interest in multi core and multiprocessors architectures, since an overall speedup can be obtaining by lowering the clock frequency and distributing processing.

LITERATURE REVIEW

Aristides Efthymiou(2004) presented a novel, low-energy content addressable memory (CAM)structure is presented which achieves an approximately four-fold improvement in energy per access. It exploits the address patterns commonly found in application programs, where testing the four least significant bits of the tag is sufficient to determine over 90% of the tag mismatches; the proposed CAM checks those bits first and evaluates the remainder of the tag only if they match. The energy savings come at the cost of a 25% increase in search time, the proposed CAM organization also supports a parallel operating mode without a speed loss but with reduced energy savings.

Chi-Shang Lin (2003) presented a novel VLSI architecture for a fully parallel pre computation-based content-addressable memory (PB-CAM) with low-power, low-cost, and low-voltage features. This design is based on a pre computation approach that saves not only power consumption of the CAM system, but also reduces transistor count and operating voltage of the CAM cell.. With a 128 words by 30 bits CAM size, the measurement results indicate that the proposed circuit works up to 100 MHz with power consumption of 33 mW at 3.3-V supply voltage and works up to 30 MHz under 1.5-V supply voltage.

Oleksiy Tyshchenko (2008) presented a match-line (ML) sensing scheme that distinguishes a match from a miss by first shunting every ML with a fixed negative resistance, then exciting the MLs with an initial charge, and subsequently observing their voltage developments. This scheme can approach the minimum possible energy consumption level for match-line sensing and implemented, in 0.18 nm CMOS, a ternary the CAM includes a pipelined search-line architecture that can reduce the SL portion of CAM power by up to 50%.

Oleksiy Tyshchenko and Ali Sheikholeslami (2008) presented a match-line (ML) sensing scheme that distinguishes a match from a miss by first shuntingevery ML with a fixed negative resistance. The initial excitation charge on the ML's can be as low as the noise level in the system, this scheme can approach the minimum possible energy consumption level for match-line sensing. The measured results confirm the power savings of the proposed sensing scheme. In addition, the CAM includes a pipelined search-line (SL) architecture that can reduce the SL portion of CAM power by up to 50%. Po-Tsang Huang and Wei Hwang (2011) proposedTCAM design utilizes two power gating techniques, namely supercut-off power gating and multi-mode data-retention power gating, to reduce theincreasing leakage power in advanced technologies.An energy-efficient 256× 144 TCAM macro is implemented using UMC 65 nm CMOS technology, and the

experimental results demonstrate a leakage power reduction of 19.3% and an energy metric of the TCAM macro of 0.165 fJ/bit/search.

Rajendra Katti et al (2003) proposed an elements of finite field GF(2m) in a ring which multiplication is more efficient.It leads to faster multipliers with a modest increase in the number of XOR and AND gates needed to construct the multiplier.The advantage is efficient systolic implementation of a multiplier for elements.Anto bennet et al.,(2015) presented application drivers and Computer-Aided Design (CAD) for 3-D Integrated Circuits (ICs).Interconnect-rich applications especially benefit, sometimes up to the equivalent of two technology nodes. This paper presents physical-design case studies of Ternary Content-Addressable Memories(TCAMs), First-In First-Out (FIFO) memories, and a 8192-point Fastfourier Transform (FFT) processor in order to quantify the benefitof the through-silicon vias in an available 180nm 3-D process.The TCAM shows a 23% power reduction and the FFT shows a22% reduction in cycle-time, coupled with an 18% reduction in energy per transform. Anto bennet et al.,(2015) proposed an wave pipelining method of high performance circuit design which implements pipelining in logic without the use of intermediate latches or registers.The advantage is reduce the chip's size and high performance.Anto bennet et al.,(2014) proposed an Cryptography for secure purposes in electronic devices.It occupy small area,consume low power in this algorithm.

PROPOSED SYSTEM

HIGH EFFICIENT CAM

A new techniques are proposed to reduce the power consumption and increase the speed. This can be achieved by using gated power ML technique and parity bit respectively. Since all available words in the CAMs are compared in parallel, result can be obtained in a single clock cycle. Experimental results show that the proposed techniques can effectively reduce power consumption in network routers and other applications.

The ability of the designs to work at low supply voltage, by re-implementing the designs in convention alone is of 65-nm technology .It demonstrates poor adaptability to voltage scaling. They cannot be operated at a supply voltage lower than 0.9 V. In proposed work CMOS 45-nm technology is used. This increases the number of transistors in the chip and the performance can be increased. This technique also reduces the chip area consumption. This is said to be integration in VLSI. The power consumption can also be reduced when compared to the conventional CAM.Proposed design can be implemented by using Tanner tool. This transform the ideas into designs it should be simulate large circuits quickly and with a high degree of accuracy. This provides fast, accurate and precise options to enable optimal balance of accuracy and performance. Enables to link from syntax errors to the SPICE deck by double clicking shown in fig 1.

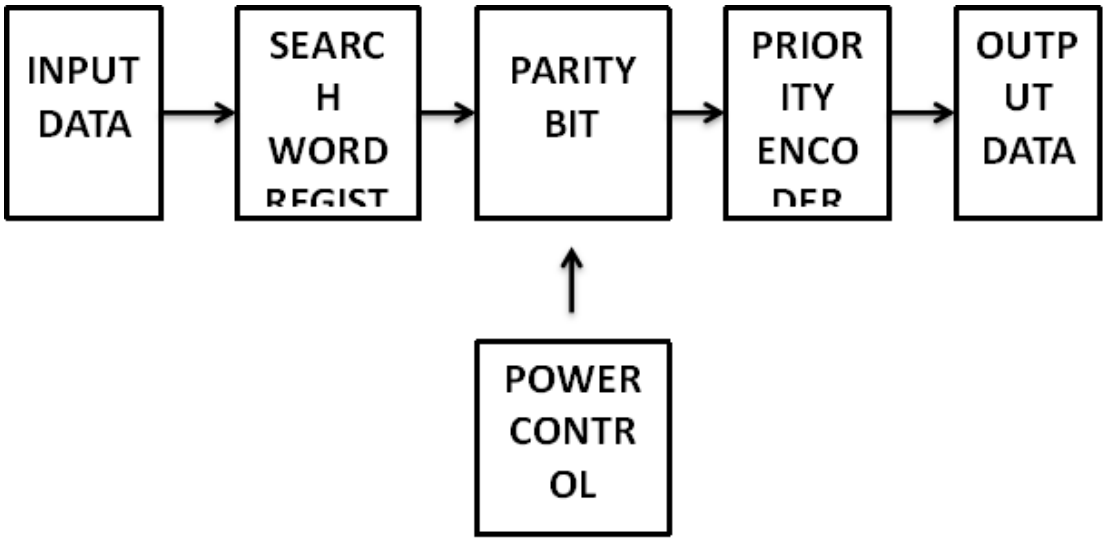

Fig 1 High Efficient CAM

ISSN: 0975-8585

INPUT DATA

The input data given in the CAM can be of the data by which the location of the data can be identified. The input can be stored in the CAM cells. These CAM cells are formed by the intersection of rows and columns.

SEARCH WORD REGISTER

A compare operation by loading an n-bit input search word into the search data register. The search data are then broadcast into the memory banks through n pairs of complementary search-lines SL and directly compared with every bit of the stored words using comparison circuits. Each stored word has a ML that is shared between its bits to convey the comparison result.

PARITY BIT

The parity bit based CAM design is consisting of the original data segment and an extra one-bit segment, derived from the actual data bits. We only obtain the parity bit, i.e., odd or even number of "1"s as shown in fig 2. The obtained parity bit is placed directly to the corresponding word and ML. Thus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage as in conventional CAM. Hence, the use of this parity bits does not improve the power performance.

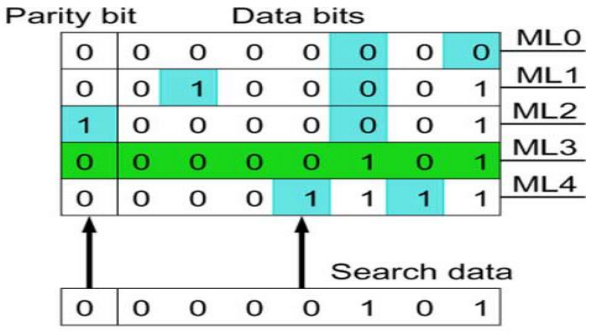

Fig 2 Parity-bit based CAM.

MATCH LINE

A match-line (ML) sensing scheme that distinguishes a match from a miss by first shunting every ML with a fixed negative resistance, then exciting the MLs with an initial charge, and subsequently observing their voltage developments. It is shown that the voltage on the matched ML will grow to VDD, as in an unstable system, whereas the voltage on a missed ML will decay to zero, as in a stable system. Since the initial excitation charge on the ML's can be as low as the noise level in the system, this scheme can approach the minimum possible energy consumption level for match-line sensing.

MATCH-LINE ENERGY CONSUMPTION

The energy consumed in a CAM is due to the repeated pre charging and discharging of all but one of the match lines in each access. This is due to the "parallel" (or NOR type) implementation of the match operation . "Serial" (or NAND type) CAM designs search one bit at a time (for each row) so that they do not discharge a single large capacitance when there is no match. They are generally slower than parallel CAMs, as their search speed depends on the number of cells in a row. This can be exploited by a mixed, serial-parallel, matching method, where after searching a small number of bits serially, the remainder can be evaluated in parallel, for those lines that could still match.

ISSN: 0975-8585

GATED-POWER ML SENSE AMPLIFIER DESIGN

The CAM cells are organized into rows (word) and columns (bit). Each cell has the same number of transistors as the conventional P-type NOR CAM and use a similar ML structure. However, the comparison unit, i.e., transistors M1,M4 and the "SRAM" unit are independently operated.The VDD is independently controlled by a power transistor Px as shown in fig 3 and a feedback loop that can auto turn-off the current to save power. The purpose of having two separate power rails of is to completely isolate the SRAM cell from any possibility of power disturbances during compare cycle.

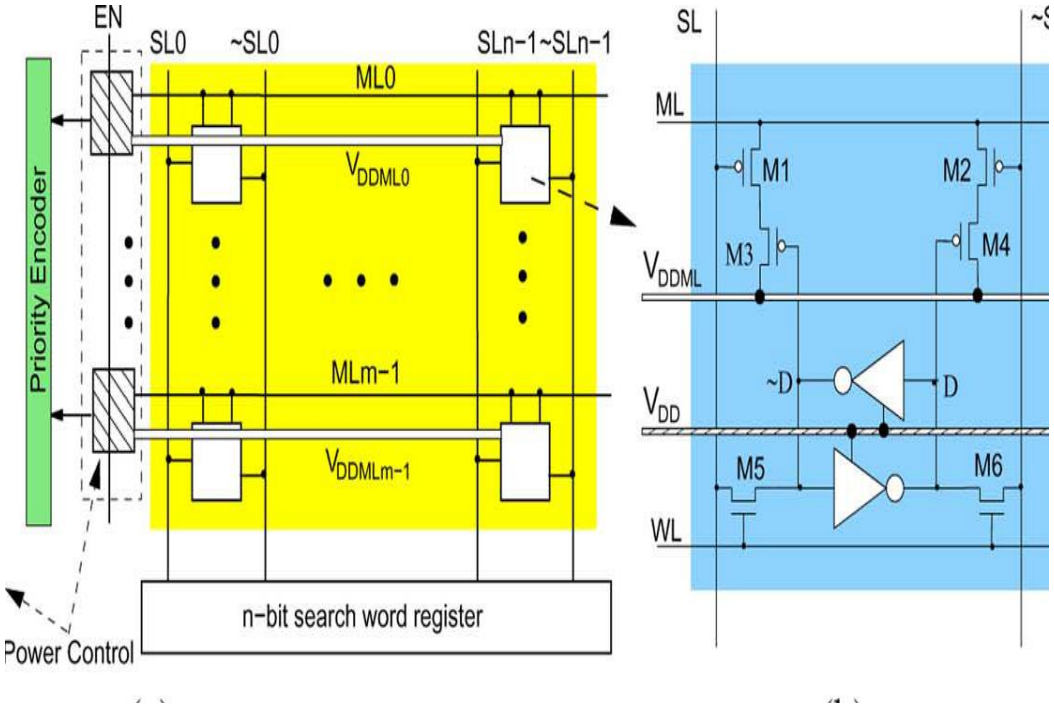

Fig 3 Proposed CAM architecture

PRIORITY ENCODER

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupt requests by acting on the highest priority request. Two or more inputs are given at the same time, the input having the highest priority will take precedence. An example of a single bit 4 to 2 encoder is shown in fig 4, where highest-priority inputs are to the left and "x" indicates an irrelevant value - i.e. any input value there yields the same output since it is superseded by higher-priority input. The output V indicates if the input is valid.

	I_3I_2	I_1	I_0	O_1	O_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

Fig 4. 4 to 2 Priority Encode

OUTPUT DATA

The output data can be obtained from the priority encoder. This chooses the best data which is matched with the input given to the CAM cells. The mismatched data at the output can be ignored by the priority encoder. Even sometimes the data which is of nearest match to the input can be accessed where no exact match is obtained.

SEARCH LINE

In the routing process in VLSI and PCB, the "gridless router" has been considered where the routing is executed without using a grid. The improved line search algorithm is one of the gridless routers where the line search algorithm is extended so that the route search procedure is executed on a linear memory space in a polynomial time. The search of the route with the minimum bends is ensured. However, the algorithm has a problem in that the route is obtained by iterating the search of the two-dimensional figures.

The associative memory presents an algorithm for the improved line search using the associative memory where the time and space complexity is *O(n)*. The proposed algorithm is implemented on the associative processor and the result is compared to the result of implementation on the general-purpose computer.

SEARCH-LINE ENERGY CONSUMPTION

Traditional CAM cells combine the search lines with the bit lines. This causes an increase in the capacitance of each search line as an extra transistor drain per cell is present (though it could be shared in the cell layout. Even after separating search and bit lines, driving the search lines accounts for almost half of the energy in search operations .Apart from having a relatively high capacitance, in parallel CAMs, one search line per bit switches at every search, even when the same value is searched each time. This is because the search lines must be driven low while the match lines are being pre-charged to avoid a direct short-circuit from supply to ground through the cells that do not match. On the other hand, serial CAMs form chains of transistors that propagate a value when all the cells match; evaluation is coordinated by pre-charging the intermediate nodes so that the search lines do not have to be pre-charged for every search.

POWER GATING TRANSISTORS:

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling power gating affects design architecture more than clock gating.

This increases time delays, as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes.

DYNAMIC POWER CONSUMPTION

The power-gated transistor is turned off after the output is obtained at the sense amplifier, the proposed technique renders a lower average power consumption. This is mainly due to the reduced voltage swing on the ML bus. Another contributing factor to the reduced average power consumption is that the new design does not need to pre charge the ML buses because the EN signal turns off transistor P_X of each row and hence the SL buses do not need to be pre-charged, which in turn saves power on the SL buses.

ISSN: 0975-8585

RESULTS AND DISCUSSIONS

Table 1 Voltage and power consumption of existing

PARAMETER	INPUT VOLTAGE	NUMBER OF TRANSISTORS	POWER CONSUMED
90nm Technology	1.8V	572	$1.77*10^{-2}$
65nm Technology	1V	572	$4.43*10^{-3}$

PROPOSED METHOD

Table 2 Voltage and power consumption of proposed

PARAMETER	INPUT VOLTAGE	NUMBER OF TRANSISTORS	POWER CONSUMED
45nm Technology	0.8V	845	$4.43*10^{-6}$

In existing method 65nm and 90nm technology is used. The power and voltage values are shown in table 1.In proposed method 45nm technology is used whose power consumption is low as shown in table 2.The input voltage is less than other technologies. Conventional Memory is a memory cells which can provide the content of data if the memory address is provided. Since if we know the memory address the data can be searched from the memory cells. Thus it increases the complexity of memory bank. Even the usage of conventional memory, delay is raised. Due to the delay, power consumption of memory banks have been raised. Thus in order to overcome the complexities CAM is introduced. CAM is an acronym of Content Addressable Memory. CAM cells are used in network routers and data compressors. As this CAMs are faster than other hardware and software search system.CAM cells are grouped together to form CAM array. If we provide the data, memory address can be accessed. Thus simultaneously we can update the content of data present in various memory sites. Thus CAM reduce the delay .Obviously, the power consumption can be reduced by CAM. CAM is based on 65nm technology by which each CAM is inbuilt with 10transistors each. Whereas if we use 90nm technology can inbuilt with 11 transistors. It provide series of CAM cells arranged in matrix form. The matrixform comprises m number of rows and n number of columns. By average, CAM array consists of 784 transistors.

BLOCK DIAGRAM of 65nm TECHNOLOGY

The CAM arrays are powered with voltage sources asshown in fig 5.Each row of CAM array is provided with individual sources.Each CAM cell in the array consists of 10 transistors.Finally, all the CAM array are fed to the encodershown in fig 6.

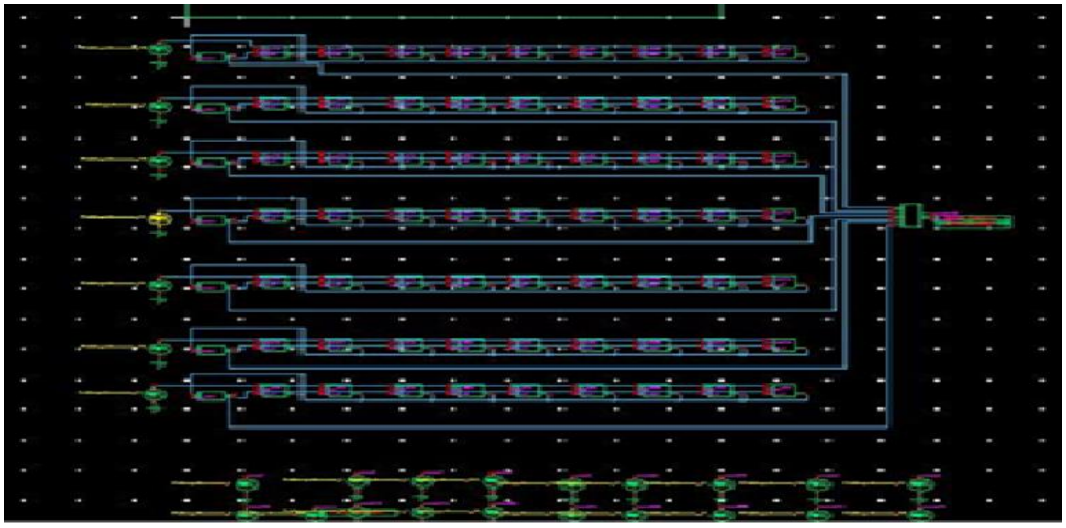

Fig 5 Block Diagram of 65nm technology

ISSN: 0975-8585

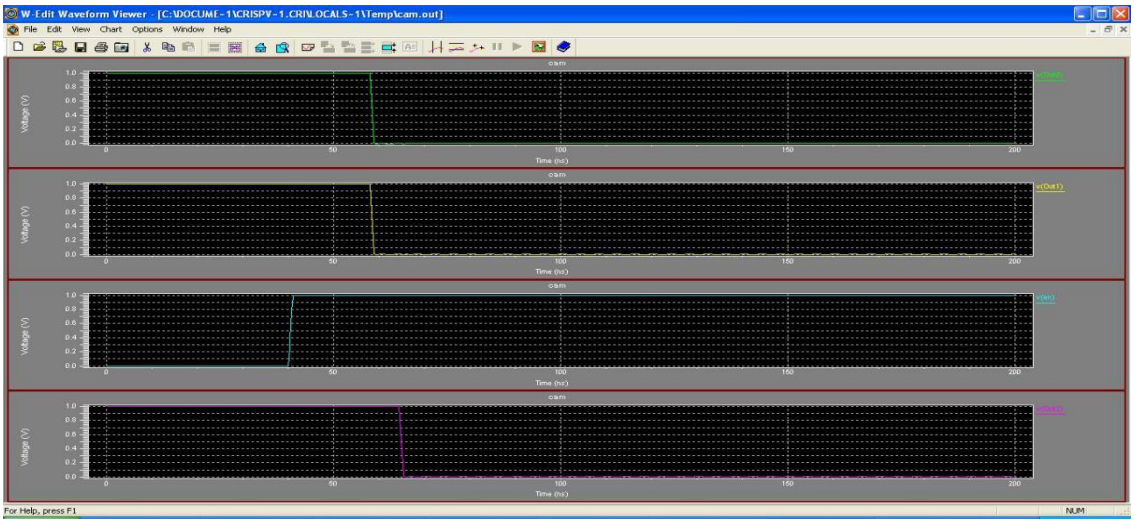

Fig 6 Output waveform of 65nm technology

BLOCKDIAGRAM of 45nm TECHNOLOGY

The CAM cell in the array consists of 9 transistors, which reduces the power consumption compared to the 65nm technology. The enable signal used to control each CAM array independently as shown in fig 7&8..

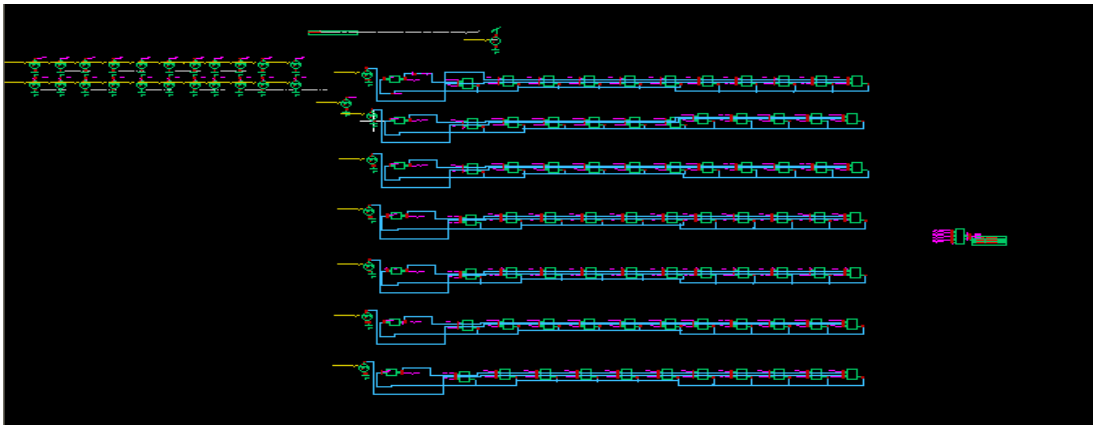

Fig 7 Block diagram of 45nm technology

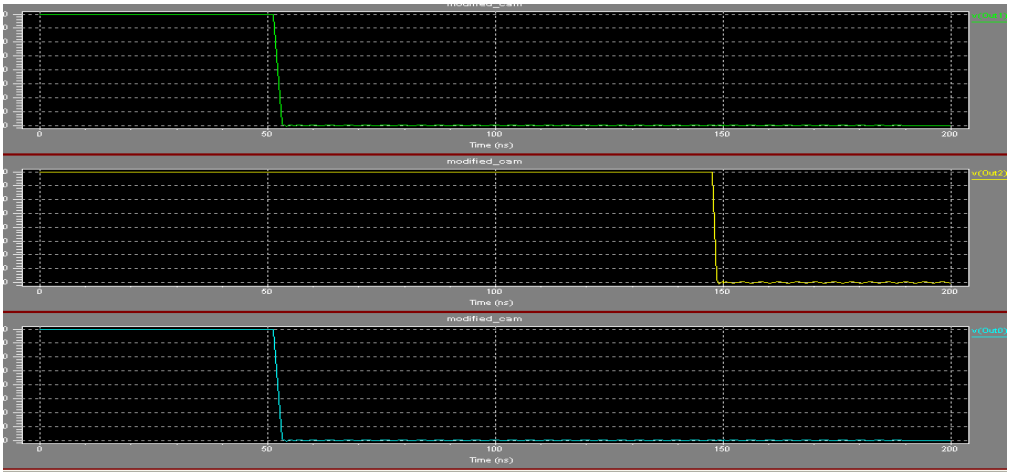

Fig 8. Output waveform of 45nm

ISSN: 0975-8585

CONCLUSION

An effective gated-power technique and a parity-bit based architecture that offer several major advantages, namely reduced peak current (and thus IR drop), average power consumption, boosted search speed and improved process variation tolerance. It is much more stable than recently published designs while maintain their low-power consumption property. When compared to the conventional design, its stability is degraded only at extremely low supply voltages. At 1 V operating condition, both designs are equally stable with no sensing errors . The design is implemented in sub-45-nm CMOS technologies which consumes power as low at the range of 4.43×10^{-6}.In this paper low power consumption and speed can be implemented. The proposed design has a smaller pull-up current due to the gated-power transistor P_x and hence sometimes error happens. In future work error can be reduced based on feedback loop structure and decisions are made at the very beginning of the sensing cycle.

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